Futurebus+ PWB/Module General Design Specification

DOCUMENT IDENTIFIER: A-SP-ELMF757-00-0000 Rev A, 22-Jan-1992

ABSTRACT: This document establishes the design and performance requirements for a rigid multilayer printed-wiring board with controlled impedance using the Futurebus+ corner.

APPLICABILITY: The purpose of this document is to specify the requirements for the Futurebus+ PWB/module design.

STATUS: APPROVED 22-Jan-1992; use VTX SMC for current status.

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CONTENTS

1 PURPOSE 1
1.1 SCOPE 1
1.2 ORDER OF PRECEDENCE 1

2 DESIGN RULES 1
2.1 10-LAYER BOARD 1
2.1.1 Board Thickness 1
2.1.2 Board Size 1
2.1.3 Routing Density 1
2.1.3.1 FB+ Corner 1
2.1.3.2 User Area 1
2.1.4 Hole and Pad Sizes 2
2.1.4.1 FB+ Corner 2
2.1.4.2 Connector Area 2
2.1.4.3 User Area 2
2.1.5 Board Layup 2
2.1.6 Conductor Width and Spacing 2
2.1.6.1 FB+ Corner 2
2.1.6.2 User Area 3
2.1.6.3 Suggested Line Widths and Impedances 3
2.2 8-LAYER BOARD 4
2.2.1 Board Thickness 4
2.2.1.1 Board Size 4
2.2.2 Routing Density 4
2.2.2.1 FB+ Corner 4
2.2.2.2 User Area 4
2.2.3 Hole and Pad Sizes 4
2.2.3.1 FB+ Corner 4
2.2.3.2 Connector Area 4
2.2.3.3 User Area 5
2.2.4 Board Layup 5
2.2.5 Conductor Width and Spacing 5
2.2.5.1 FB+ Corner 5
2.2.5.2 User Area 5
2.2.5.3 Suggested Line Widths and Impedances 6
2.3 6-LAYER BOARD 6
2.3.1 Board Thickness 6
2.3.2 Board Size 6
2.3.3 Routing Density 6
2.3.3.1 FB+ Corner 6
2.3.3.2 User Area 7
2.3.4 Hole and Pad Sizes 7
2.3.4.1 FB+ Corner 7
2.3.4.2 Connector Area 7

2.3.4.3 User Area 7
2.3.5 Board Layup 8
2.3.6 Conductor Width and Spacing 8
2.3.6.1 FB+ Corner 8
2.3.6.2 User Area 8
2.3.6.3 Suggested Line Widths and Impedances 8

3 ELECTRICAL REQUIREMENTS 9
3.1 CHARACTERISTIC IMPEDANCE 9
3.2 EQUIPMENT 9
3.3 HIPOT TEST POINTS 9
3.4 SHORTS OPENS TEST 9

4 MATERIALS 10
4.1 SOLDERMASK 10
4.1.1 Soldermask Color 10
4.2 WARPAGE 10

Appendix A REFERENCED DOCUMENTS 11

A.1 EL-Class Digital Documents 11

TABLES

1 Summary of Component Hole and Signal Via Sizes, 10-Layer Board 2
2 Recommended Line Width, 10-Layer Board 3
3 Suggested Line Widths, 10-Layer Board 3
4 Summary of Component Hole and Signal Via Sizes, 8-Layer Board 5
5 Recommended Line Width, 8-Layer Board 5
6 Suggested Line Widths, 8-Layer Board 6
7 Summary of Component Hole and Signal Via Sizes, 6-Layer Board 7
8 Recommended Line Width, 6-Layer Board 8
9 Suggested Line Widths, 6-Layer Board 9

1 PURPOSE

This document specifies the requirements for Futurebus+ (FB+) PWB/Module design.

1.1 SCOPE

This document establishes the design and performance requirements for rigid multilayer printed-wiring boards with controlled impedance using the Futurebus+ corner.

1.2 ORDER OF PRECEDENCE

In the event of a conflict between the text of this specification and references cited herein, the text of this specification shall take precedence. The text of this specification shall not be interpreted to reduce the requirements of *DEC STD 176 Printed Wiring Board Acceptance Criteria* (all sections) or *DEC STD 030 Module Manufacturing Standard* (all sections), but shall be interpreted to be in addition to all sections of DEC STD 176 and DEC STD 030.

2 DESIGN RULES

Drawings referenced in the following paragraphs can be found in either *PC Engineering Handbook—Standard Circuit and Finger Details*, order no. EL-ENPCB-01, or *PC Engineering Handbook—Layer Construction Drawings*, order no. EL-ENPCB-02.

2.1 10-LAYER BOARD

2.1.1 Board Thickness

Finished board thickness shall meet the requirements of Layer Construction D-MD-ELEN648-0-DBU.

2.1.2 Board Size

The finished board size shall be 289.35 mm (11.392 inch) by 264.85 mm (10.427 inch). See Layer Construction D-MD-ELEN654-0-DBU for details.

2.1.3 Routing Density

2.1.3.1 FB+ Corner

The design may allow for one line between all hole diameters on 1.27 mm (0.050 inch) grid, and one line between all hole diameters on 2.00 mm (0.079 inch) grid. The minimum spacing between any two patterns shall be no less than 0.177 mm (0.007 inch).

2.1.3.2 User Area

The design may allow for two lines between all hole diameters on 1.27 mm (0.050 inch) grid, and for three lines between all hole diameters on 2.54 mm (0.100 inch) grid. The design may allow for one line between all hole diameters on 2.00 mm (0.079 inch) grid. The minimum spacing between any two patterns shall be no less than 0.127 mm (0.005 inch), 0.178 mm (0.007 inch) is preferred.

2.1.4 Hole and Pad Sizes

2.1.4.1 FB+ Corner

The pad size for holes of 0.381 mm (0.015 inch) diameter shall be 0.76 mm (0.030 inch) on inner layers, and 0.71 mm (0.028 inch) on L1 and L10 (Side 1 and 2).

2.1.4.2 Connector Area

The pad size for connector holes of 0.76 mm (0.030 inch) diameter shall be 1.27 mm (0.050 inch) on all layers.

2.1.4.3 User Area

The pad size for hole diameter 1.067 mm (0.042 inch) shall be 1.524 (0.060 inch) on all layers. The pad size for holes of 0.381 mm (0.015 inch) diameter shall be 0.76 mm (0.030 inch) on all layers, except L10 (Side 2) which shall be 0.889 mm (0.035 inch) pads. See Table 1.

Table 1: Summary of Component Hole and Signal Via Sizes, 10-Layer Board

Feature	PTH Diameter	Pad Diameter	Clearance Size
Hole	0.965 mm to 1.092 mm (0.038 inch to 0.043 inch)	1.524 mm (0.060 inch)	1.778 mm (0.070 inch)
	0.685 mm to 0.838 mm (0.027 inch to 0.033 inch)	1.27 mm (0.050 inch)	1.524 mm (0.060 inch)
Via	0.00 mm to 0.406 mm [1] (0.00 inch to 0.016 inch)		1.016 mm (0.040 inch)

[1]Layer 1 shall have 0.76 mm (0.030 inch) pads, except in the FB+ corner which shall have 0.71 mm (0.028 inch). Layers 2, 5, 6, and 9 shall have 0.76 mm (0.030 inch) pads. Layer 10 shall have 0.76 mm (0.030 inch) pads, except in the FB+ corner which shall have 0.71 mm (0.028 inch).

2.1.5 Board Layup

See Layer Construction D-MD-ELEN648-0-DBU for layup requirement.

2.1.6 Conductor Width and Spacing

2.1.6.1 FB+ Corner

The minimum lateral spacing of internal layer conductors shall be not less than 0.177 mm (0.007 inch). The minimum lateral spacing of conductors on outer layers (Side 1 and 2) shall be not less than 0.152 mm (0.006 inch).

Table 2: Recommended Line Width, 10-Layer Board

Layer Number	Line Impedance and Width—70 Ohm
Layer 1	0.254 mm (0.010 inch)
Layer 5	0.152 mm (0.006 inch)
Layer 6	0.152 mm (0.006 inch)
Layer 10	0.254 mm (0.010 inch)

2.1.6.2 User Area

The minimum lateral spacing of internal and external layer conductors shall be not less than 0.127 mm (0.005 inch), 0.178 mm (0.007 inch) preferred. The minimum lateral width of internal and external conductors shall be not less than 0.127 mm (0.005 inch).

2.1.6.3 Suggested Line Widths and Impedances

See Table 3 for suggested line widths and impedances.

Table 3: Suggested Line Widths, 10-Layer Board

Layer	Line Impedance and Width					
Number	50 ohm	56 ohm	60 ohm	63 ohm	67 ohm	70 ohm
L1	0.406 mm (0.016 inch)	0.355 mm (0.014 inch)	0.330 mm (0.013 inch)	0.304 mm (0.012 inch)	0.279 mm (0.011 inch)	0.279 mm (0.011 inch)
L2	0.305 mm (0.012 inch)	0.254 mm (0.010 inch)	0.229 mm (0.009 inch)	0.203 mm (0.008 inch)	0.177 mm (0.007 inch)	0.152 mm (0.006 inch)
L5	0.305 mm (0.012 inch)	0.254 mm (0.010 inch)	0.229 mm (0.009 inch)	0.203 mm (0.008 inch)	0.177 mm (0.007 inch)	0.152 mm (0.006 inch)
L6	0.305 mm (0.012 inch)	0.254 mm (0.010 inch)	0.229 mm (0.009 inch)	0.203 mm (0.008 inch)	0.177 mm (0.007 inch)	0.152 mm (0.006 inch)
L9	0.305 mm (0.012 inch)	0.254 mm (0.010 inch)	0.229 mm (0.009 inch)	0.203 mm (0.008 inch)	0.177 mm (0.007 inch)	0.152 mm (0.006 inch)
L10	0.406 mm (0.016 inch)	0.355 mm (0.014 inch)	0.330 mm (0.013 inch)	0.304 mm (0.012 inch)	0.279 mm (0.011 inch)	0.279 (0.011 inch)

2.2 8-LAYER BOARD

2.2.1 Board Thickness

Finished board thickness shall meet the requirements of Layer Construction D-MD-ELEN647-0-DBU.

2.2.1.1 Board Size

The finished board size shall be 289.35 mm (11.392 inch) by 264.85 mm (10.427 inch). See Layer Construction D-MD-ELEN654-0-DBU for details.

2.2.2 Routing Density

2.2.2.1 FB+ Corner

The design may allow for one line between all hole diameters on 1.27 mm (0.050 inch) grid, and one line between all hole diameters on 2.00 mm (0.079 inch) grid. The minimum spacing between any two patterns shall be no less than 0.177 mm (0.007 inch).

2.2.2.2 User Area

The design may allow for two lines between all hole diameters on 1.27 mm (0.050 inch) grid, and for three lines between all hole diameters on 2.54 mm (0.100 inch) grid. The design may allow for one line between all hole diameters on 2.00 mm (0.079 inch) grid. The minimum spacing between any two patterns shall be no less than 0.127 mm (0.005 inch), 0.178 mm (0.007 inch) is preferred.

2.2.3 Hole and Pad Sizes

2.2.3.1 FB+ Corner

The pad size for holes of 0.381 mm (0.015 inch) diameter shall be 0.76 mm (0.030 inch) on inner layers, and 0.71 mm (0.028 inch) on L1 and L8 (Side 1 and 2).

2.2.3.2 Connector Area

The pad size for connector holes of 0.76 mm (0.030 inch) diameter shall be 1.27 mm (0.050 inch) on all layers.

2.2.3.3 User Area

The pad size for hole diameter 1.067 mm (0.042 inch) shall be 1.524 (0.060 inch) on all layers. The pad size for holes of 0.381 mm (0.015 inch) diameter shall be 0.76 mm (0.030 inch) on all layers, except L8 (Side 2) which shall be 0.889 mm (0.035 inch) pads. See Table 4.

Table 4: Summary of Component Hole and Signal Via Sizes, 8-Layer Board

Feature	PTH Diameter	Pad Diameter	Clearance Size
Hole	0.965 mm to 1.092 mm (0.038 inch to 0.043 inch)	1.524 mm (0.060 inch)	1.778 mm (0.070 inch)
	0.685 mm to 0.838 mm (0.027 inch to 0.033 inch)	1.27 mm (0.050 inch)	1.524 mm (0.060 inch)
Via	0.00 mm to 0.406 mm [1] (0.00 inch to 0.016 inch)		1.016 mm (0.040 inch)

[1]Layer 1 shall have 0.76 mm (0.030 inch) pads, except in the FB+ corner which shall have 0.71 mm (0.028 inch). Layers 2, 4, 5, and 7 shall have 0.76 mm (0.030 inch) pads. Layer 8 shall have 0.76 mm (0.030 inch) pads, except in the FB+ corner which shall have 0.71 mm (0.028 inch).

2.2.4 Board Layup

See Layer Construction D-MD-ELEN647-0-DBU for layup requirement.

2.2.5 Conductor Width and Spacing

2.2.5.1 FB+ Corner

The minimum lateral spacing of internal layer conductors shall be not less than 0.177 mm (0.007 inch). The minimum lateral spacing of conductors on outer layers (Side 1 and 2) shall be not less than 0.152 mm (0.006 inch). See Table 5.

Table 5: Recommended Line Width, 8-Layer Board

Layer Number	Line Impedance and Width—70 ohm
Layer 1	0.254 mm (0.010 inch)
Layer 4	0.152 mm (0.006 inch)
Layer 5	0.152 mm (0.006 inch)
Layer 8	0.254 mm (0.010 inch)

2.2.5.2 User Area

The minimum lateral spacing of internal and external layer conductors shall be not less than 0.127 mm (0.005 inch), 0.178 mm (0.007 inch) preferred. The minimum lateral width of internal and external conductors shall be not less than 0.127 mm (0.005 inch).

2.2.5.3 Suggested Line Widths and Impedances

See Table 6 for suggested line widths and impedances.

Table 6: Suggested Line Widths, 8-Layer Board

Layer	Line Impedance and Width					
Number	50 ohm	56 ohm	60 ohm	63 ohm	67 ohm	70 ohm
L1	0.406 mm (0.016 inch)	0.355 mm (0.014 inch)	0.330 mm (0.013 inch)	0.304 mm (0.012 inch)	0.279 mm (0.011 inch)	0.279 mm (0.011 inch)
L2	0.305 mm (0.012 inch)	0.254 mm (0.010 inch)	0.229 mm (0.009 inch)	0.203 mm (0.008 inch)	0.177 mm (0.007 inch)	0.152 mm (0.006 inch)
L4	0.305 mm (0.012 inch)	0.254 mm (0.010 inch)	0.229 mm (0.009 inch)	0.203 mm (0.008 inch)	0.177 mm (0.007 inch)	0.152 mm (0.006 inch)
L5	0.305 mm (0.012 inch)	0.254 mm (0.010 inch)	0.229 mm (0.009 inch)	0.203 mm (0.008 inch)	0.177 mm (0.007 inch)	0.152 mm (0.006 inch)
L7	0.305 mm (0.012 inch)	0.254 mm (0.010 inch)	0.229 mm (0.009 inch)	0.203 mm (0.008 inch)	0.177 mm (0.007 inch)	0.152 mm (0.006 inch)
L8	0.406 mm (0.016 inch)	0.355 mm (0.014 inch)	0.330 mm (0.013 inch)	0.304 mm (0.012 inch)	0.279 mm (0.011 inch)	0.279 mm (0.011 inch)

2.3 6-LAYER BOARD

2.3.1 Board Thickness

Finished board thickness shall meet the requirements of Layer Construction D-MD-ELEN646-0-DBU.

2.3.2 Board Size

The finished board size shall be 289.35 mm (11.392 inch) by 264.85 mm (10.427 inch). See Layer Construction D-MD-ELEN654-0-DBU for details.

2.3.3 Routing Density

2.3.3.1 FB+ Corner

The design may allow for one line between all hole diameters on 1.27 mm (0.050 inch) grid, and one line between all hole diameters on 2.00 mm (0.079 inch) grid. The minimum spacing between any two patterns shall be no less than 0.177 mm (0.007 inch).

2.3.3.2 User Area

The design may allow for two lines between all hole diameters on 1.27 mm (0.050 inch) grid, and for three lines between all hole diameters on 2.54 mm (0.100 inch) grid. The design may allow for one line between all hole diameters on 2.00 mm (0.079 inch) grid. The minimum spacing between any two patterns shall be no less than 0.127 mm (0.005 inch), 0.178 mm (0.007 inch) is preferred.

2.3.4 Hole and Pad Sizes

2.3.4.1 FB+ Corner

The pad size for holes of 0.381 mm (0.015 inch) diameter shall be 0.76 mm (0.030 inch) on inner layers, and 0.71 mm (0.028 inch) on L1 and L6 (Side 1 and 2).

2.3.4.2 Connector Area

The pad size for connector holes of 0.76 mm (0.030 inch) diameter shall be 1.27 mm (0.050 inch) on all layers.

2.3.4.3 User Area

The pad size for hole diameter 1.067 mm (0.042 inch) shall be 1.524 (0.060 inch) on all layers. The pad size for holes of 0.381 mm (0.015 inch) diameter shall be 0.76 mm (0.030 inch) on all layers, except L6 (Side 2) which shall be 0.889 mm (0.035 inch) pads. See Table 7.

Table 7: Summary of Component Hole and Signal Via Sizes, 6-Layer Board

Feature	PTH Diameter	Pad Diameter	Clearance Size
Hole	0.965 mm to 1.092 mm (0.038 inch to 0.043 inch)	1.524 mm (0.060 inch)	1.778 mm (0.070 inch)
	0.685 mm to 0.838 mm (0.027 inch to 0.033 inch)	1.27 mm (0.050 inch)	1.524 mm (0.060 inch)
Via	0.00 mm to 0.406 mm [1] (0.00 inch to 0.016 inch)		1.016 mm (0.040 inch)

[1]Layer 1 shall have 0.76 mm (0.030 inch) pads, except in the FB+ corner which shall have 0.71 mm (0.028 inch). Layers 3 and 4 shall have 0.76 mm (0.030 inch) pads. Layer 6 shall have 0.76 mm (0.030 inch) pads, except in the FB+ corner which shall have 0.71 mm (0.028 inch).

2.3.5 Board Layup

See Layer Construction D-MD-ELEN646-0-DBU for layup requirement.

2.3.6 Conductor Width and Spacing

2.3.6.1 FB+ Corner

The minimum lateral spacing of internal layer conductors shall be not less than 0.177 mm (0.007 inch). The minimum lateral spacing of conductors on outer layers (Side 1 and 2) shall be not less than 0.152 mm (0.006 inch). See Table 8.

Table 8: Recommended Line Width, 6-Layer Board

Layer Number	Line Impedance and Width—70 ohm
Layer 1	0.254 mm (0.010 inch)
Layer 3	0.152 mm (0.006 inch)
Layer 4	0.152 mm (0.006 inch)
Layer 6	0.254 mm (0.010 inch)

2.3.6.2 User Area

The minimum lateral spacing of internal and external layer conductors shall be not less than 0.127 mm (0.005 inch), 0.178 mm (0.007 inch) preferred. The minimum lateral width of internal and external conductors shall be not less than 0.127 mm (0.005 inch).

2.3.6.3 Suggested Line Widths and Impedances

See Table 9 for suggested line widths and impedances.

Table 9: Suggested Line Widths, 6-Layer Board

Layer	Line Impedance and Width					
Number	50 ohm	56 ohm	60 ohm	63 ohm	67 ohm	70 ohm
L1	0.406 mm (0.016 inch)	0.355 mm (0.014 inch)	0.330 mm (0.013 inch)	0.304 mm (0.012 inch)	0.279 mm (0.011 inch)	0.279 mm (0.011 inch)
L3	0.305 mm (0.012 inch)	0.254 mm (0.010 inch)	0.229 mm (0.009 inch)	0.203 mm (0.008 inch)	0.177 mm (0.007 inch)	0.152 mm (0.006 inch)
L4	0.305 mm (0.012 inch)	0.254 mm (0.010 inch)	0.229 mm (0.009 inch)	0.203 mm (0.008 inch)	0.177 mm (0.007 inch)	0.152 mm (0.006 inch)
L6	0.406 mm (0.016 inch)	0.355 mm (0.014 inch)	0.330 mm (0.013 inch)	0.304 mm (0.012 inch)	0.279 mm (0.011 inch)	0.279 mm (0.011 inch)

3 ELECTRICAL REQUIREMENTS

3.1 CHARACTERISTIC IMPEDANCE

Controlled impedance is not necessarily a requirement of Futurebus+ (see B2999, note 22). However, many options will require controlled impedance. An impedance test strip is provided, which options may remove, relocate, or reconfigure as needed. The test strip uses a small profile SMA plug pattern (see 3.2) to minimize board space consumed. The line width in the impedance test pattern should be changed to match the predominate etch used on each layer and the following note added to the MD drawing.

NOTE

Characteristic impedance of all signal lines in the impedance test pattern shall be XX ohms ± 10% (line-to-ground). The impedance shall be measured on each trace of the test pattern that is part of the PC board.

3.2 EQUIPMENT

The SMA used for impedance testing shall be a Huber-Suhner 2-pin probe, part number 82-SMA-50-0-3 or equivalent, which is approved by Digital.

3.3 HIPOT TEST POINTS

Each mutually-isolated power or ground plane must have an identified test point for HIPOT testing.

3.4 SHORTS OPENS TEST

Circuit continuity testing of boards delivered under this specification shall be data driven. Self-learning testers shall not be be used. Test equipment used shall derive required test points from the data base.

4 MATERIALS

4.1 SOLDERMASK

Use of a permanent soldermask coating is required and shall be applied to both sides of the board. Soldermask features (pads) shall be as follows:

Circuit pad size +0.177 mm (+0.007 inch). See Table 1.

4.1.1 Soldermask Color

The color of any soldermask used on this product shall be green and must be uniform in color across the entire PWB.

4.2 WARPAGE

Warpage (bow or twist) shall be in accordance with DEC STD 176-0.

APPENDIX A REFERENCED DOCUMENTS

A.1 EL-Class Digital Documents

EL-Class Number	Document Title
EL-00030-00	*DEC STD 030 Module Manufacturing Standard*
EL-00176-00	*DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*
EL-ENPCB-01	*PC Board Engineering Handbook - Standard Circuit and Finger Details*
EL-ENPCB-02	*PC Board Engineering Handbook—Layer Construction Drawings*

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